Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.096”**

**ANODE**

**.072 X .072”**

**.096”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .072” X .072”**

**Backside Potential: Cathode**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .096” X .096” DATE: 10/19/21**

**MFG: X-REL THICKNESS .015” P/N: XTR1K1210**

**DG 10.1.2**

#### Rev B, 7/19/02